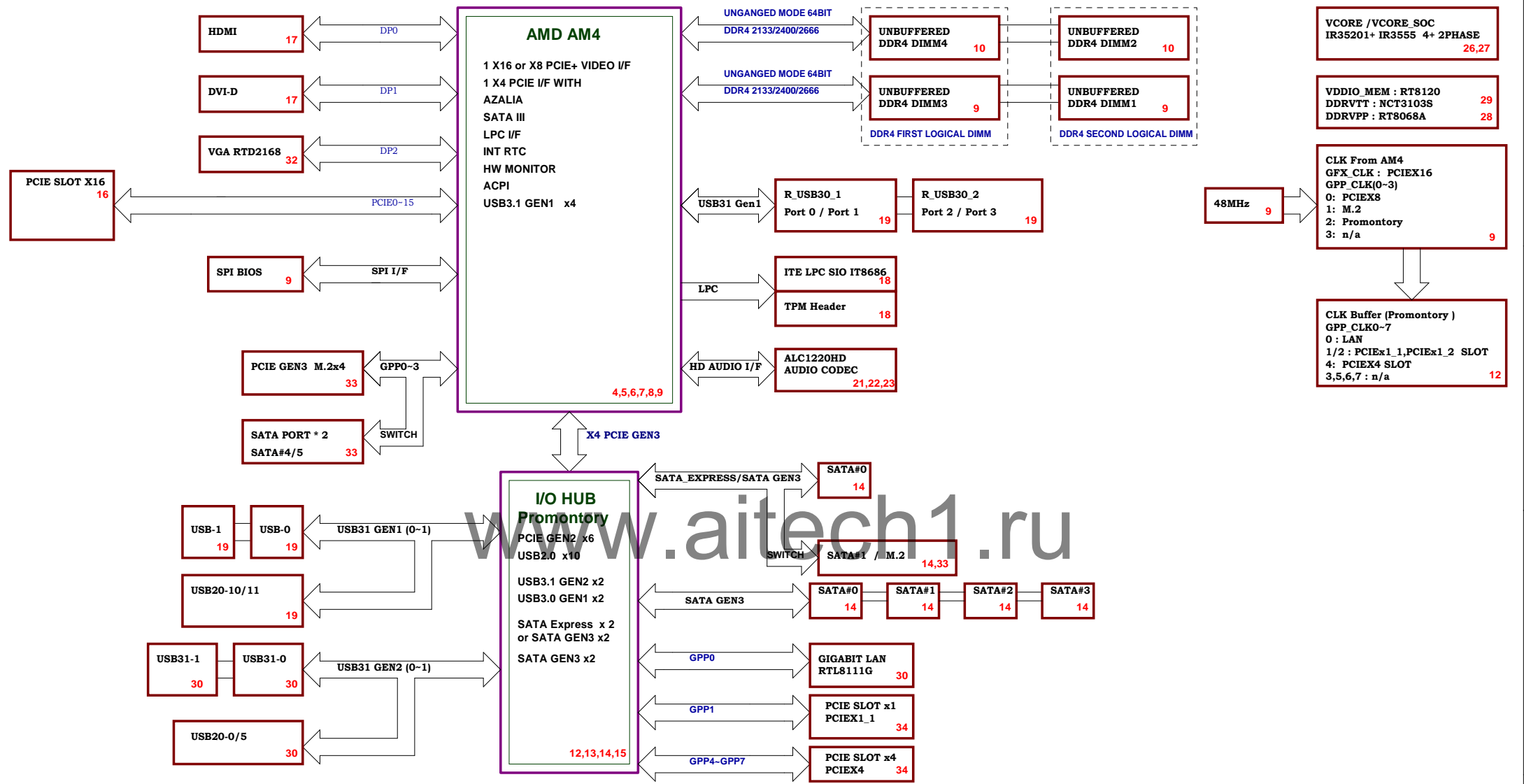


GA-AB350-GAMING 3

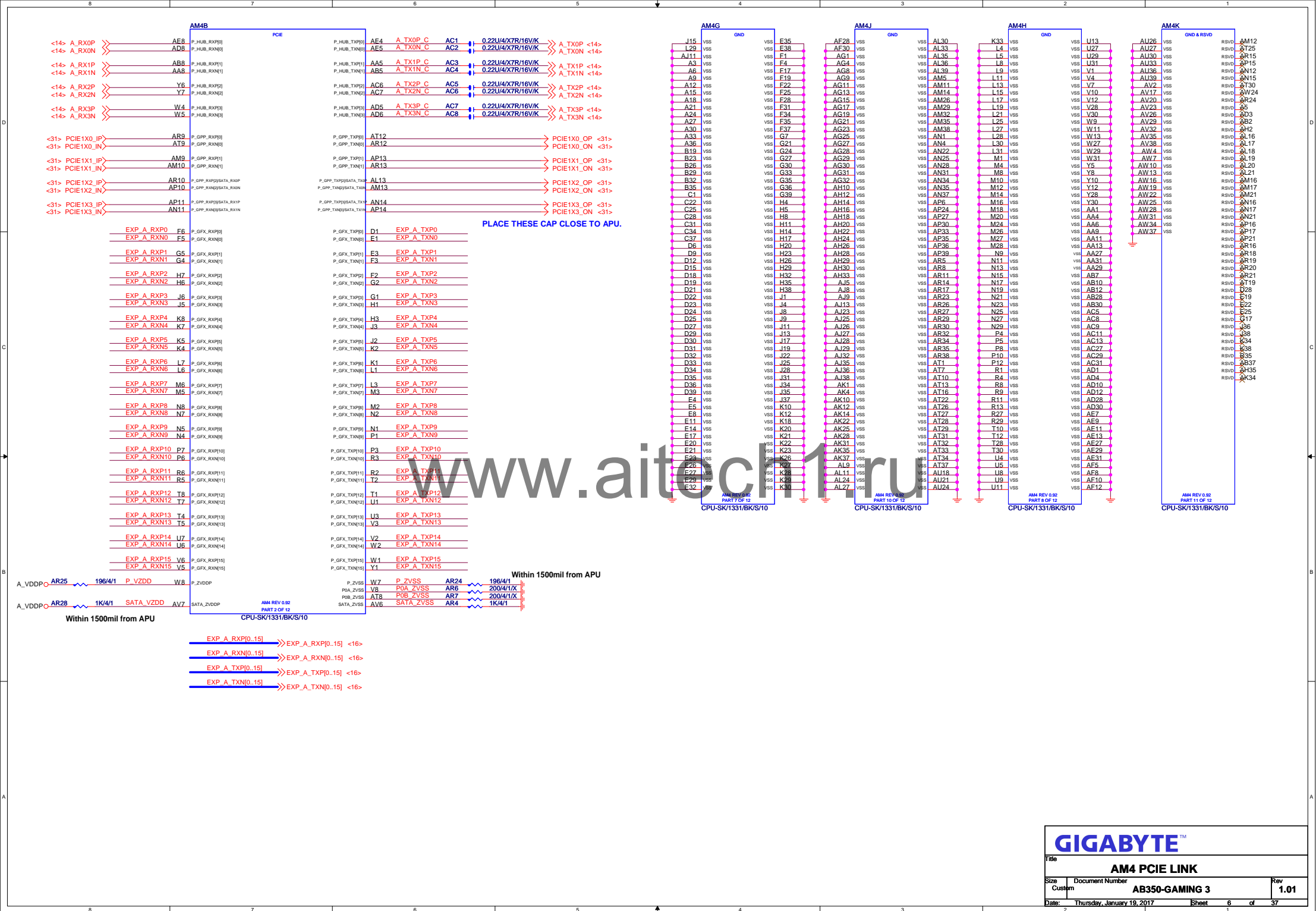
PAGE	TITLE	Revision : 1.01
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU DDR4 MEMORY	
05	CPU CONTROL	
06	CPU GFX, GPP, SB, GND	
07	CPU ACPI/GPIO/USB/AUDIO	
08	CPU POWER & GND	
09	CPU CLK/SPI/USB	
10	DDR4 CHANNEL A	
11	DDR4 CHANNEL B	
12	PM CLK, SPI, MISC	
13	PM USB	
14	PM UMI/GPP/SATA	
15	PM POWER & GND	
16	PCI EXPRESS x16	
17	HDMI , DVI	
18	IT8688CX , TPM	
19	F_USB30 , R_USB30 , F_USB20	
20	A_VDD1V8, DAC_PWR	
21	ALC1220 CODEC	
22	AUDIO JACK	
23	POWER SEQUENCE , A_VDDP	
24	PWM SL95712	
25	VCORE MOS , VCORE_SOC MOS	

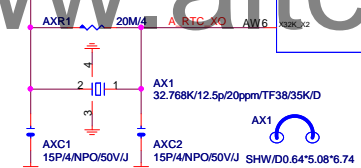
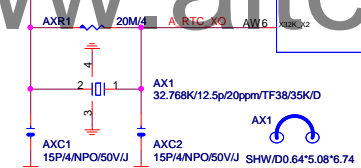
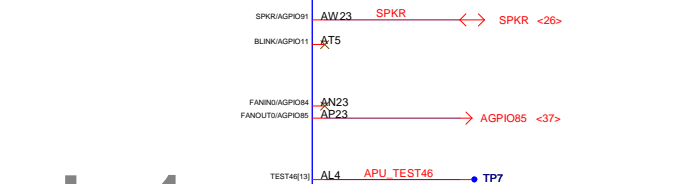
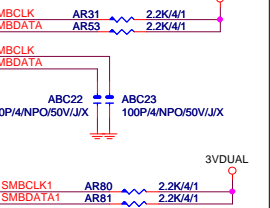
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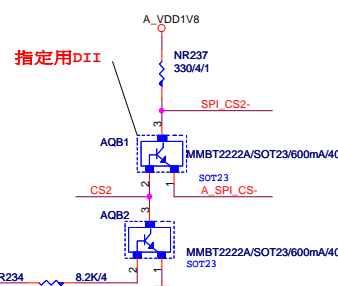
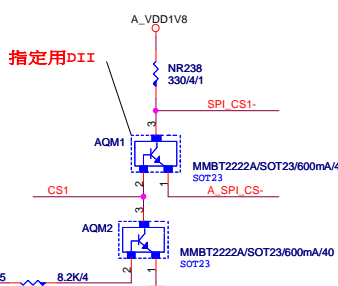
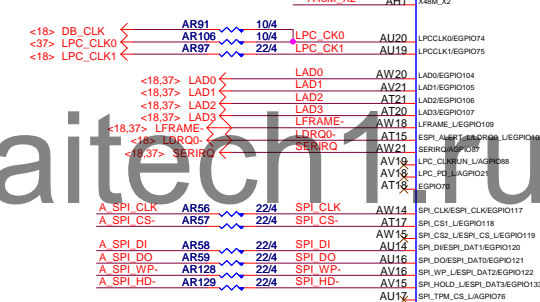
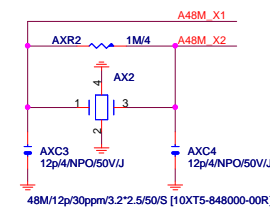
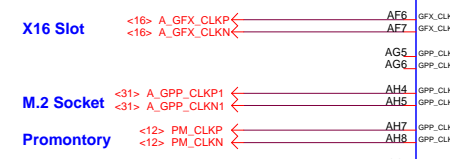
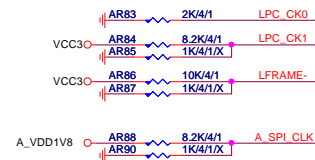


Title			
CPU CONTROL			
Size	Document Number	Rev	
Custom	AB350-GAMING 3	1.01	
Date:	Thursday, January 19, 2017	Sheet	5 of 37

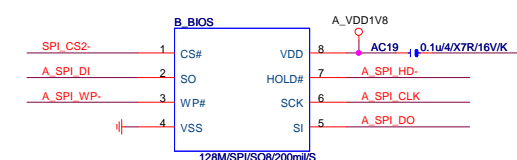
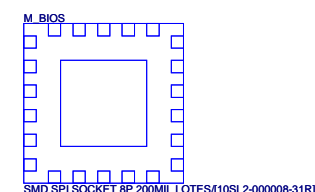
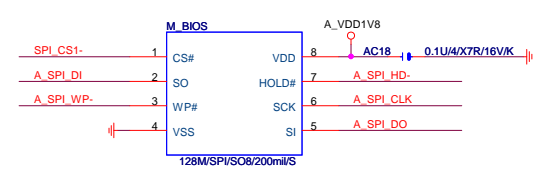
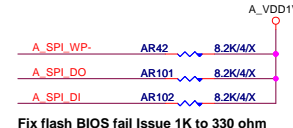


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AM4 MISC			
Title	Document Number		
Size Custom	AB350-GAMING 3		Rev 1.01
Date: Thursday, January 19, 2017	Sheet 7	of 37	



★1.8V SPI ROM USE

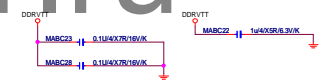
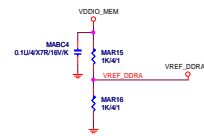
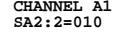
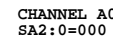


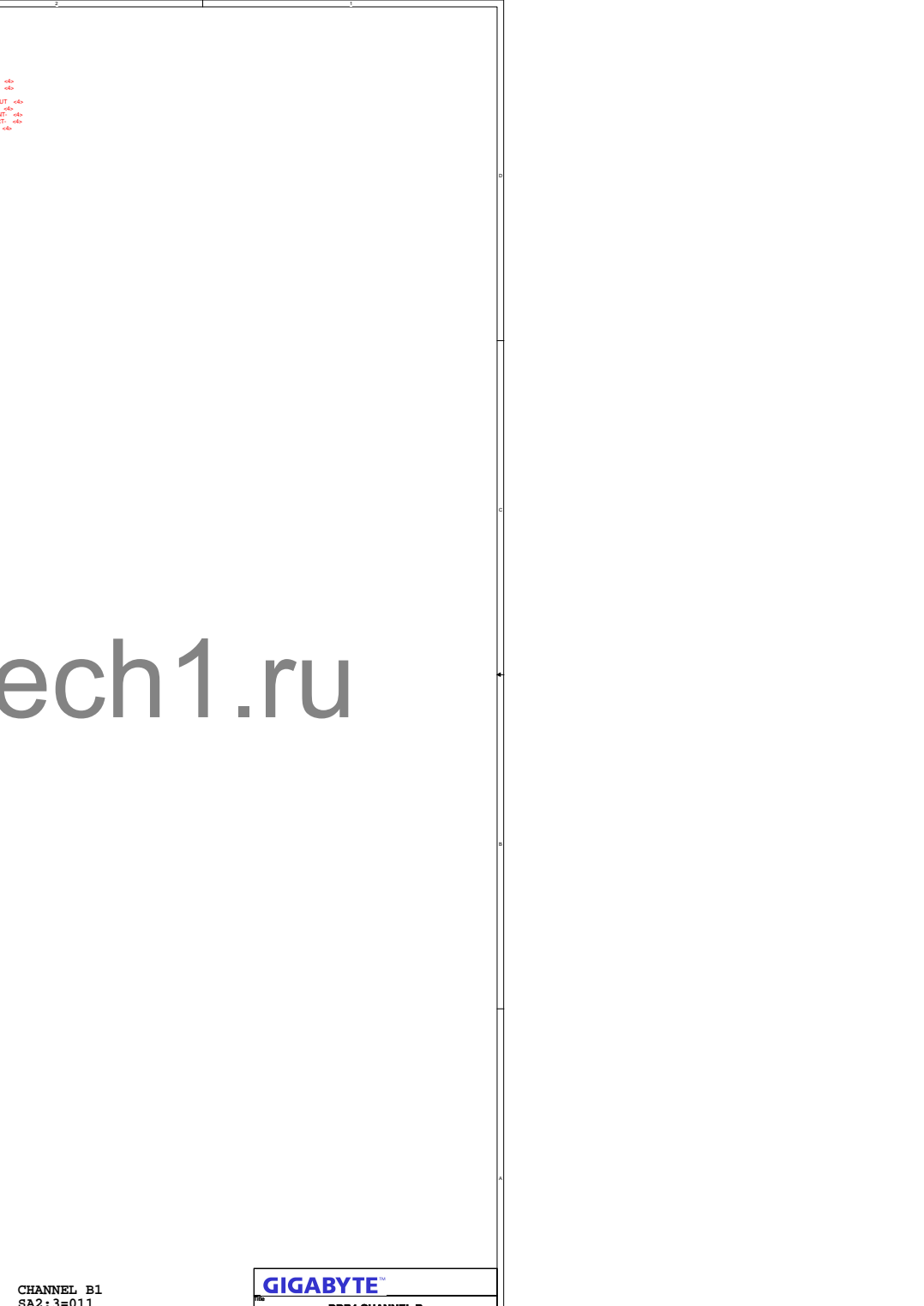
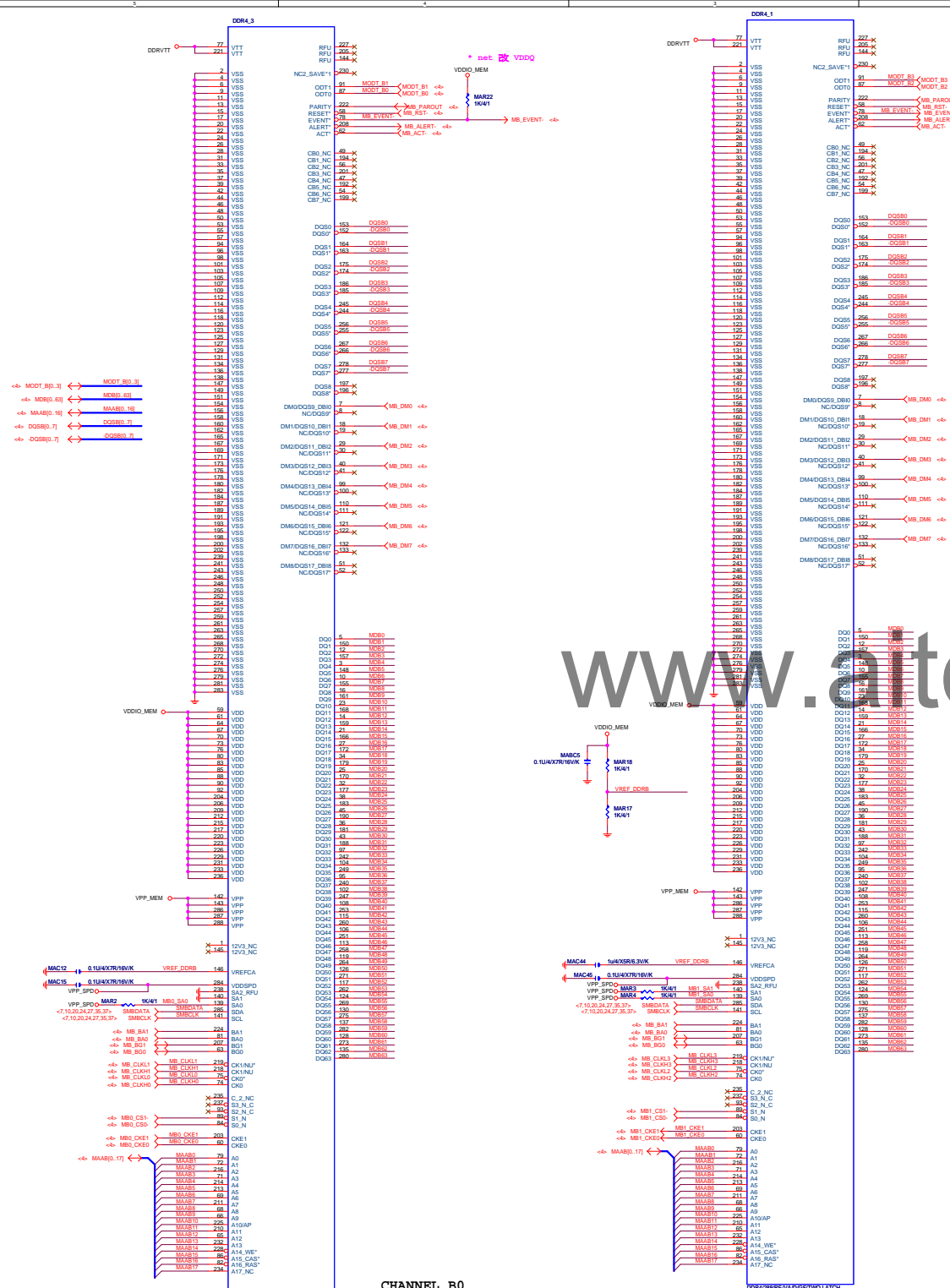
GIGABYTE

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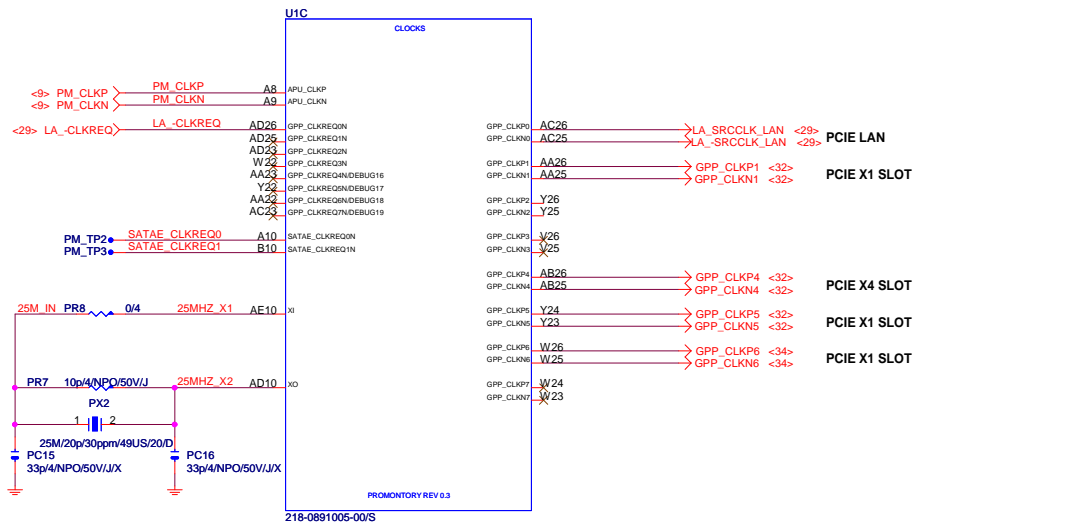
Size: Custom Document Number: **AB350-GAMING 3** Rev: **1.01**

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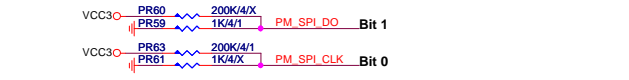


GIGABYTE		
DDR4 CHANNEL B		
File	Document Number	Rev
Size	AR350-GAMING 3	1.01
Comments		
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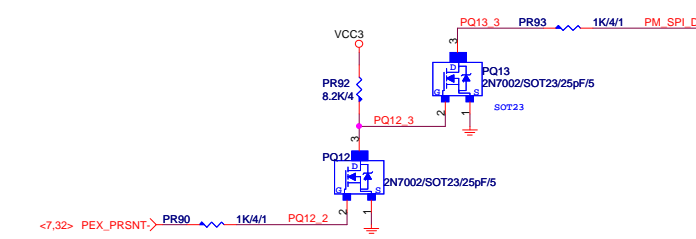
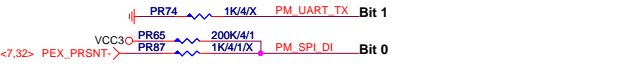


BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

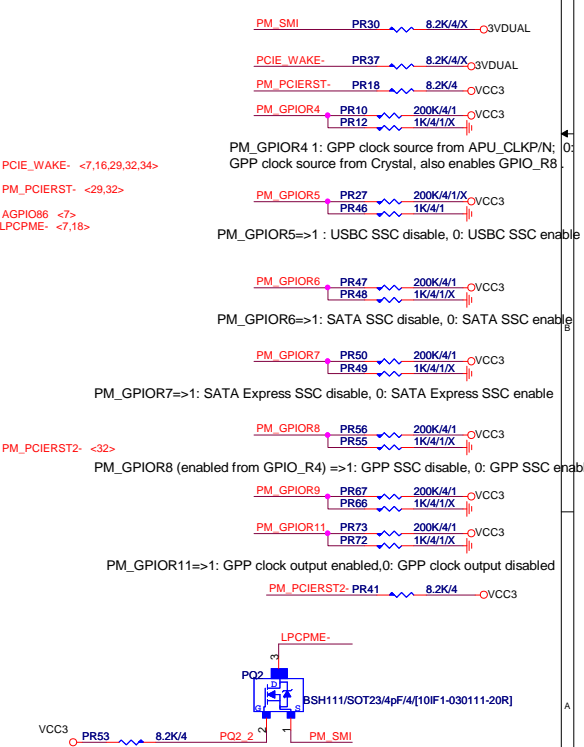
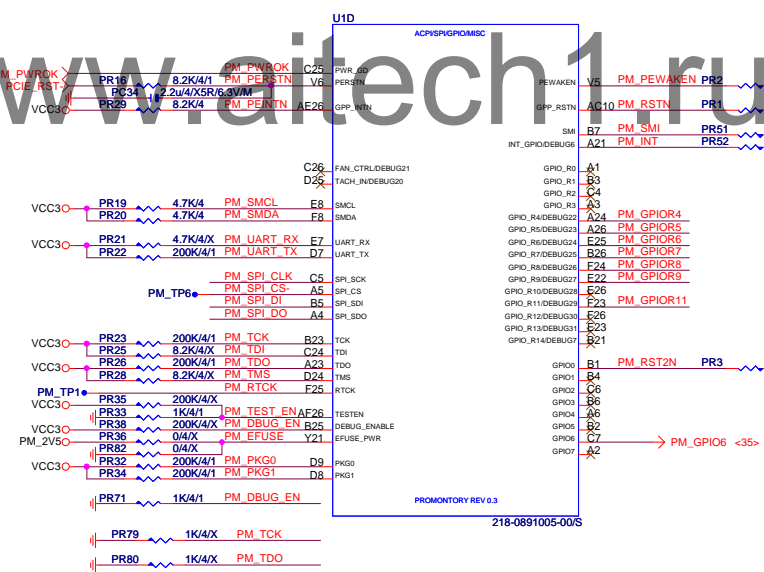
PM GPP Group 0 Strap: 11=> 1PCle x4, 10=>1PCle x2, 2PClex1, 01=>4PCle x1, 00=>Reserved.
PM GPP Group 0=>0~3



PM GPP Group 1 Strap: 11=> 1PCle x4, 10=>1PCle x2, 2PClex1, 01=>4PCle x1, 00=>Reserved.
PM GPP Group 1=>4~7



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ANS 5133386

GIGABYTETM

Title

B350 CLK GEN / GPIO

Size

Custom

Document Number

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1.01

Date:

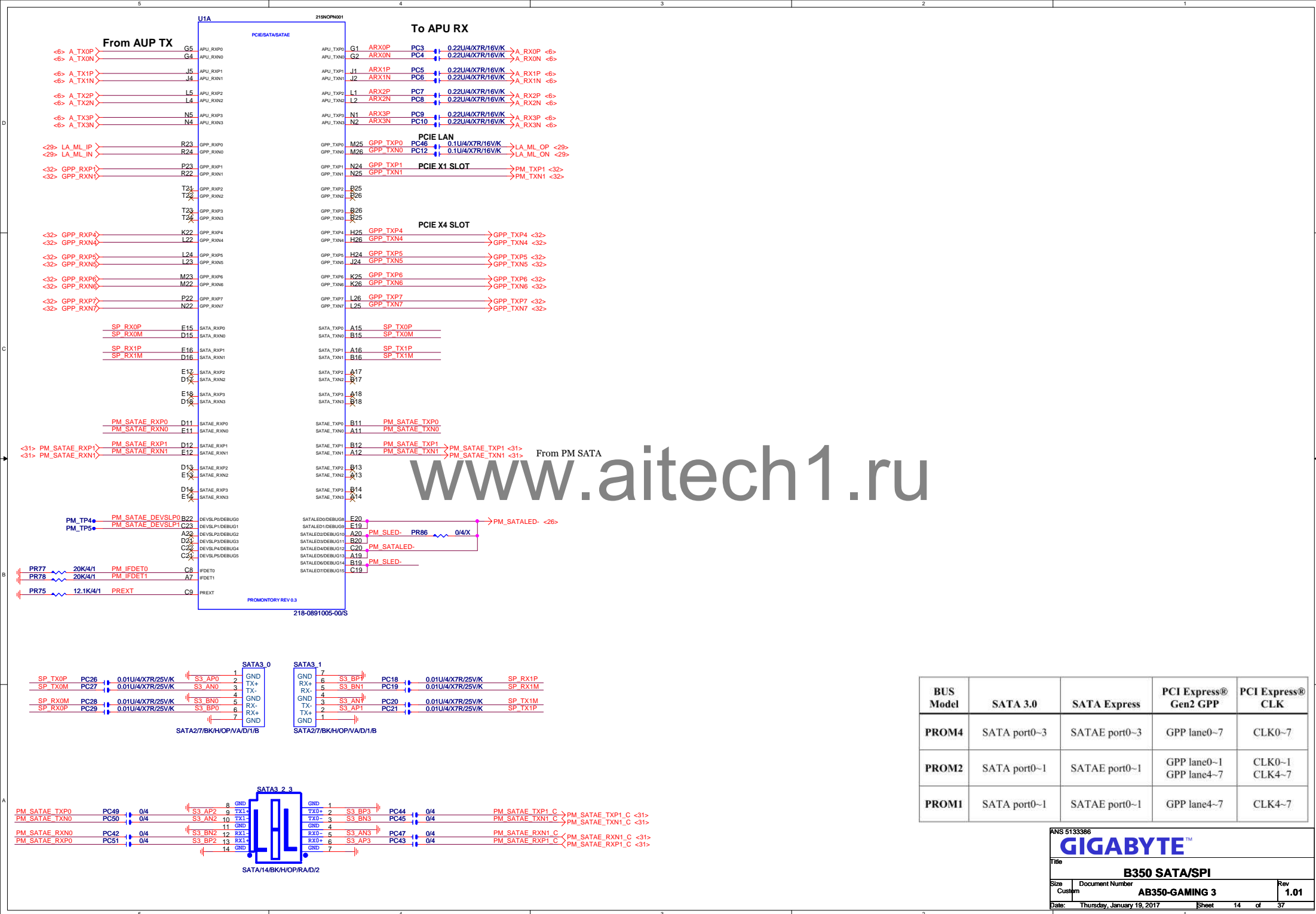
Thursday, January 19, 2017

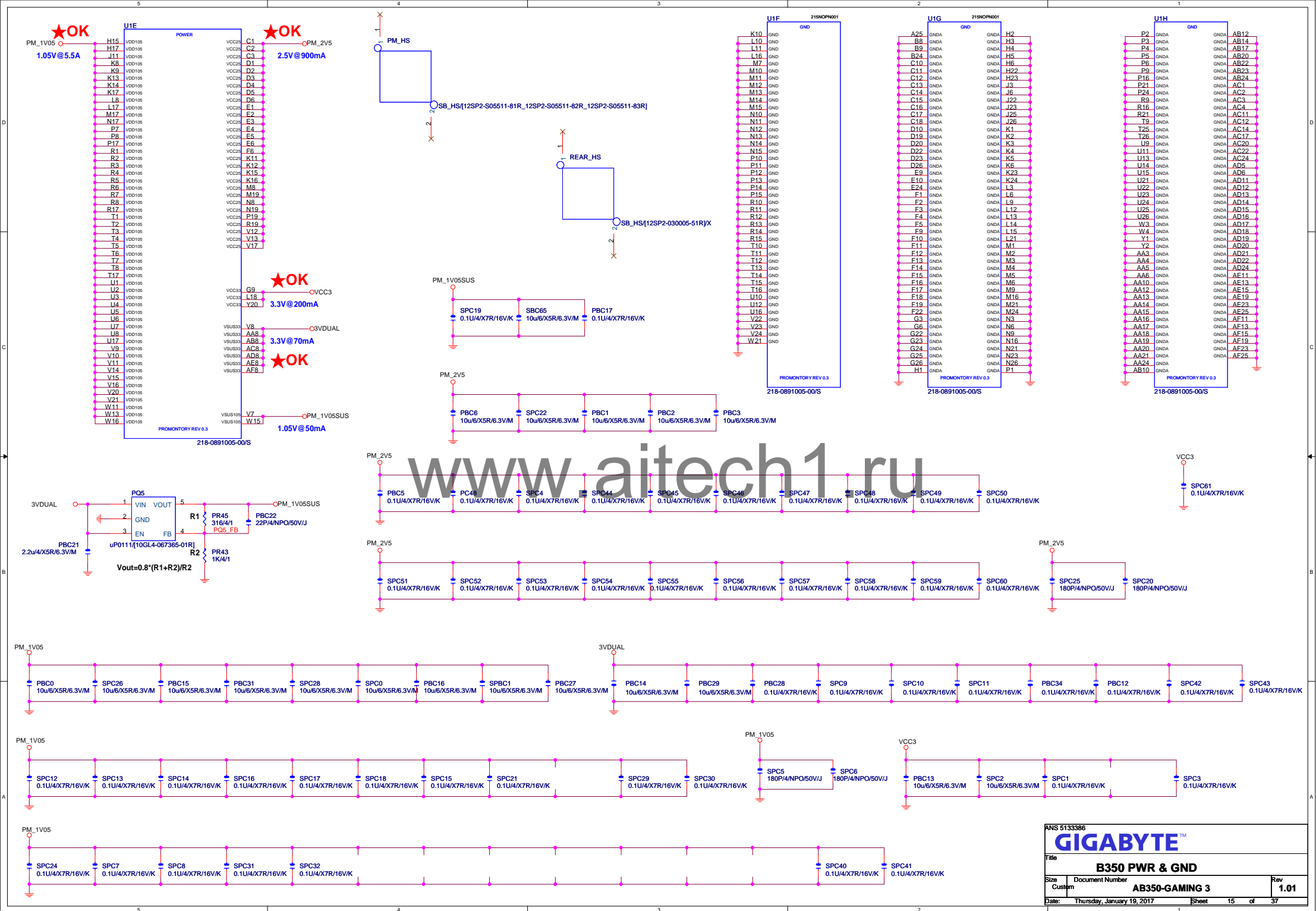
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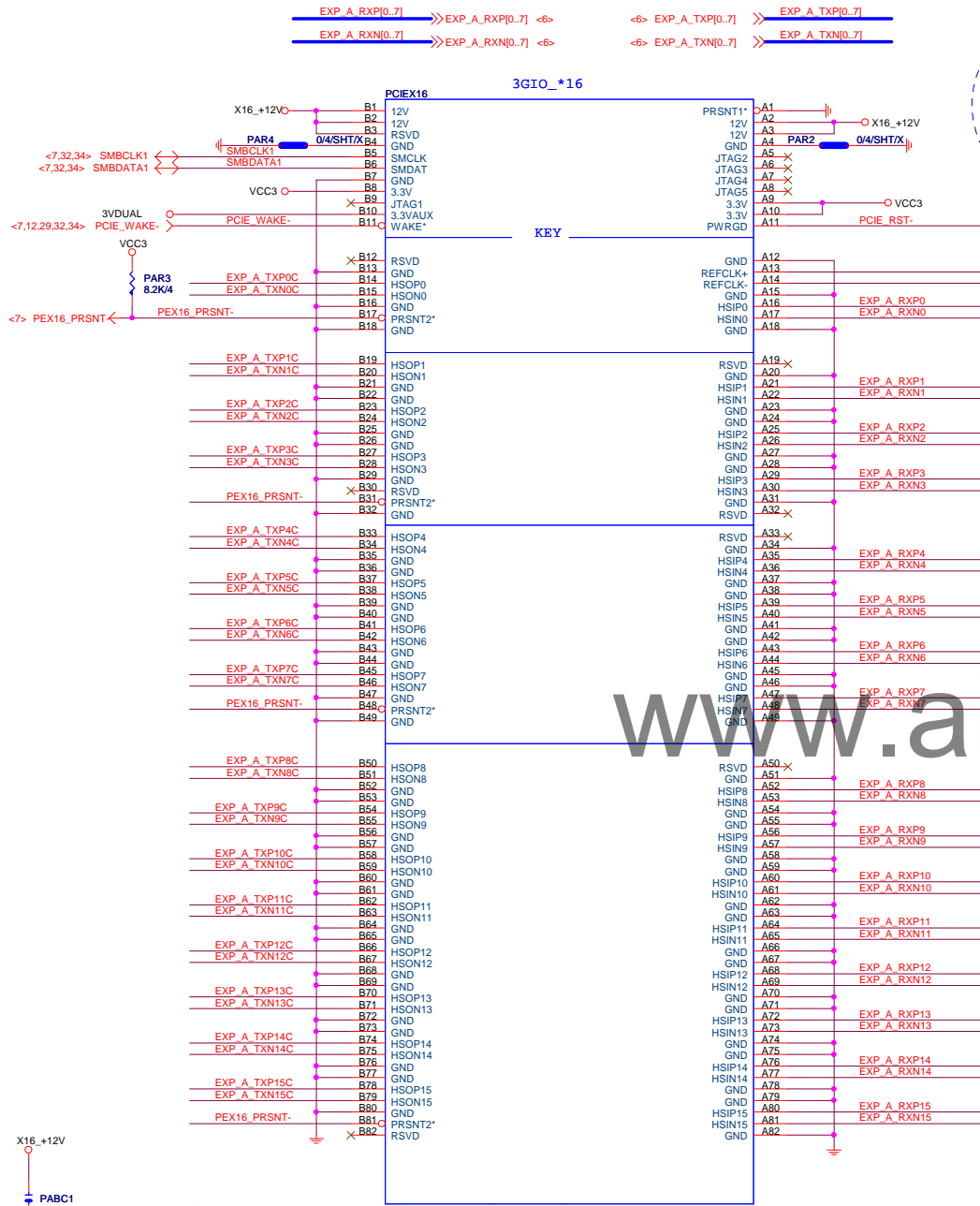
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of

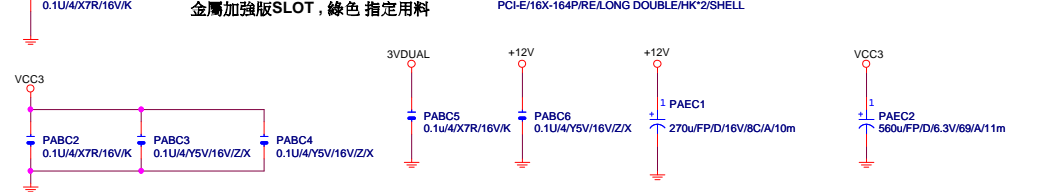
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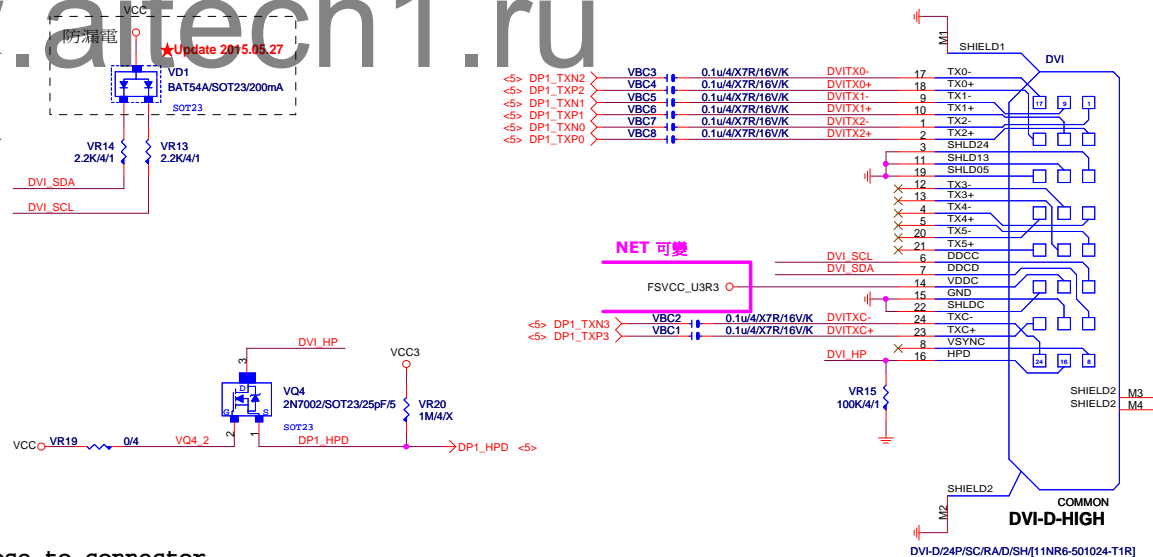
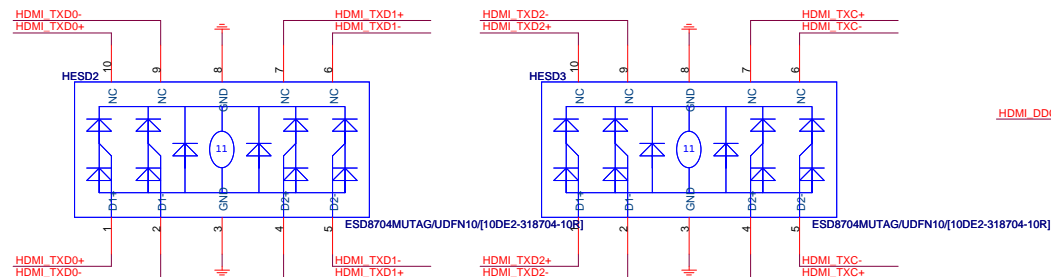


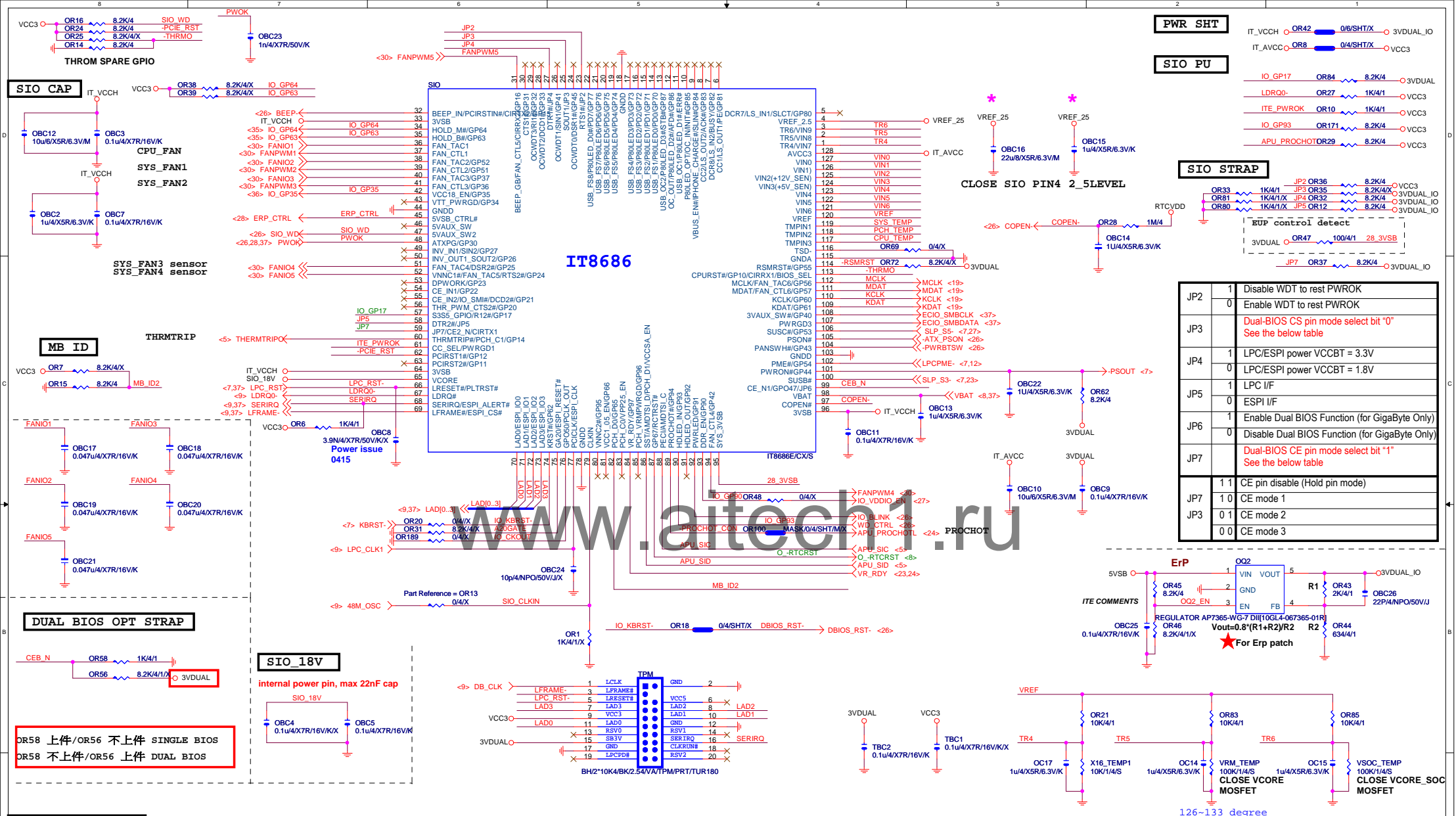




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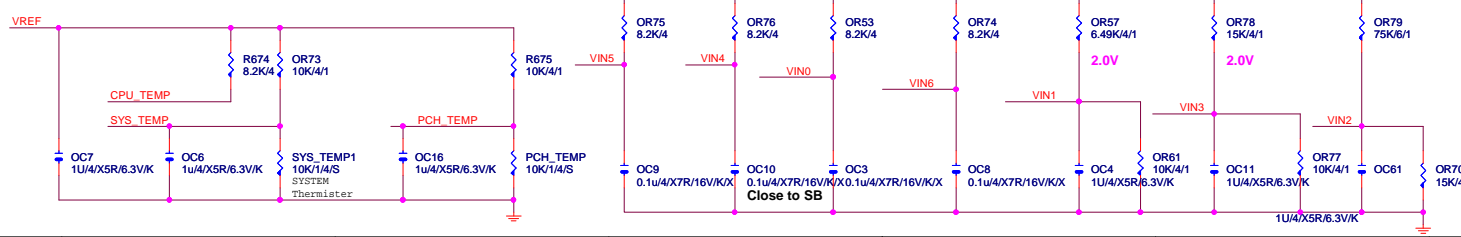






FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT_FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

Hardware Monitor circuits



ITE 8628CX , HWM , TPM , KB_MS_USB

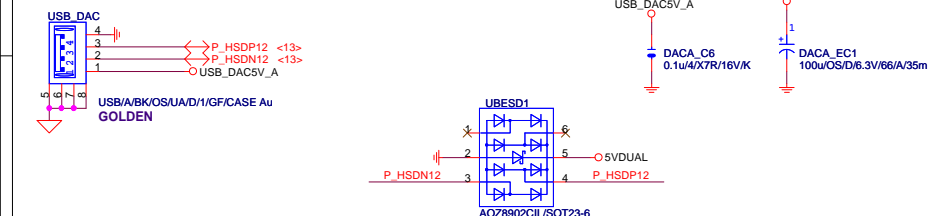
Size
Custom

Document Number
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Rev
1.01

Date: Thursday, January 19, 2017

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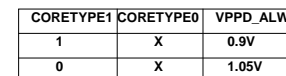
L=1u
DCR=3.2 mohm
Isat=18A
Idc=15A



* 大電容 x0



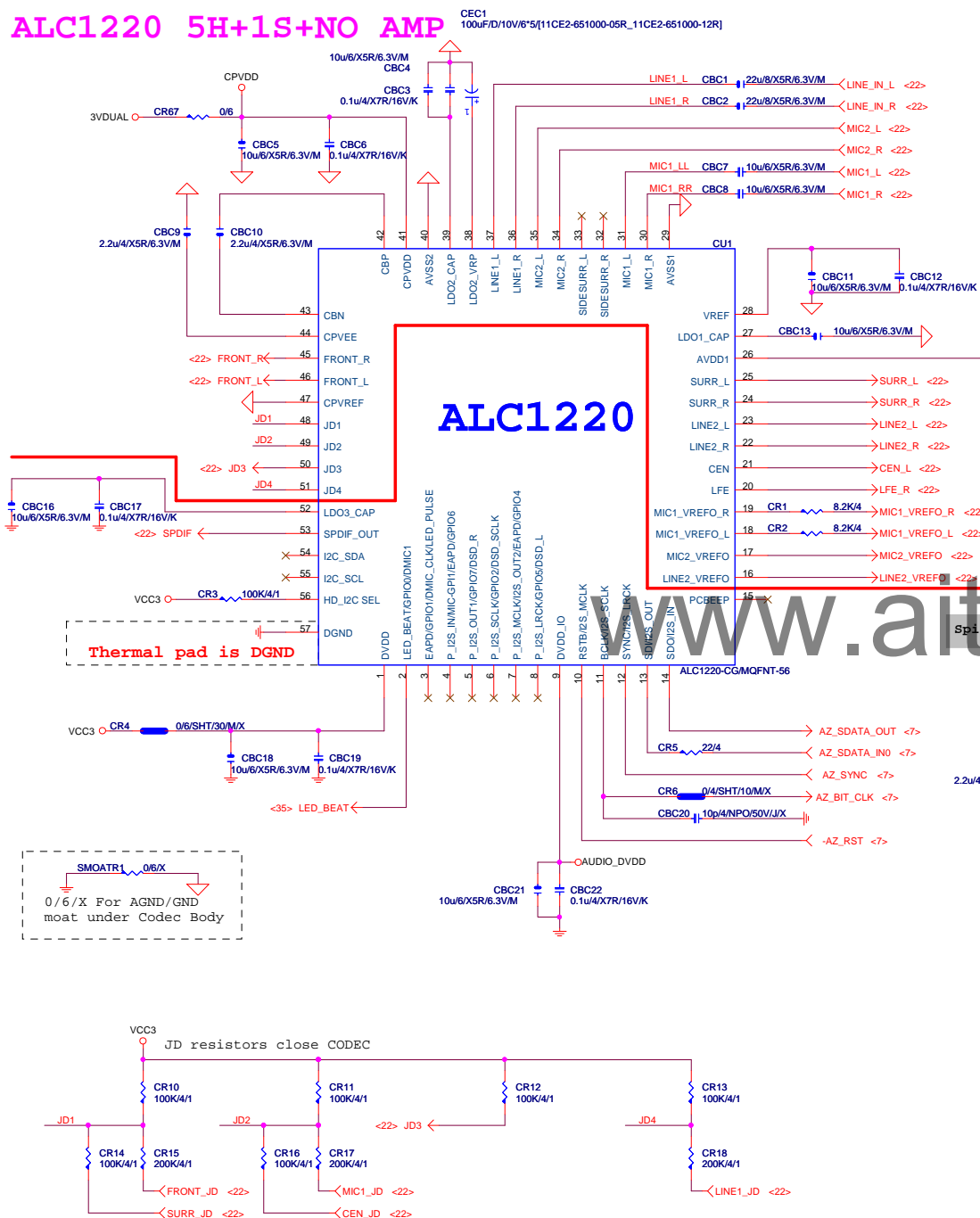
【技術通報R&D技術通報156】
RT9018(RICHTEK)與NCT3730(NUVOTON),
EM5103GE(EMC)做共用,針對PIN7(FB)分壓阻值部份
(R1/R2)須做修改為100K以上電阻值



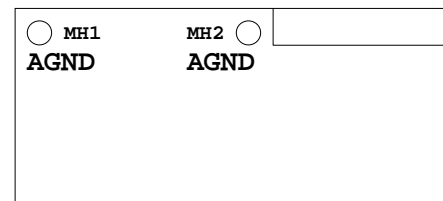
CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

Rev 0.5

ALC1220 5H+1S+NO AMP



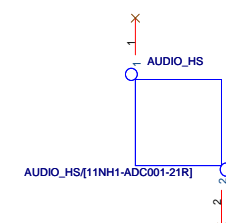
LAYOUT注意:螺絲孔下AGND方式
1. MH1,MH2全部下AGND



LAYOUT注意:是否要加?
AGND切割線



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BOM OPTION :

1. AUDIO CONNECT

不銹鋼料號:11NR6-403025-A2R

鍍金料號:11NR6-403025-92R

2. AUDIO CAP

Nichicon MW音效電容 : 11CE1-651000-12R

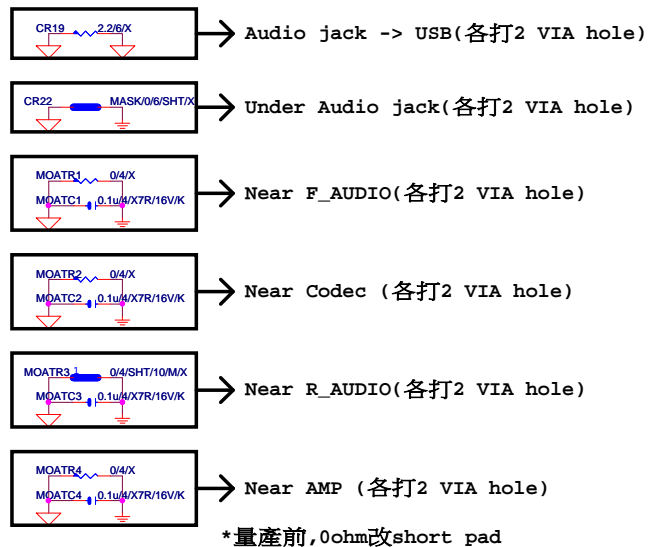
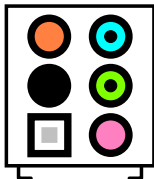
Chemicon音效電容 : 11CE2-651000-05R

GIGABYTE

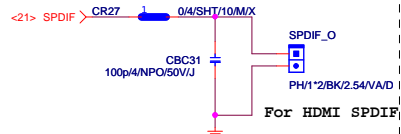
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ALC1220 CODEC		
Size	Document Number	Rev
Custom	AB350-GAMING 3	1.01
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Rev 0.5

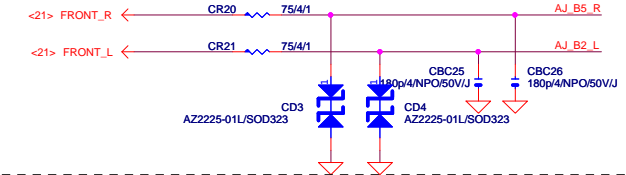
AZALIA JACK



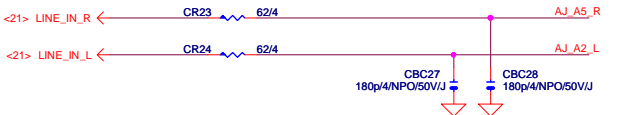
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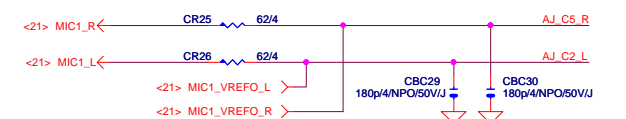
LINE-OUT



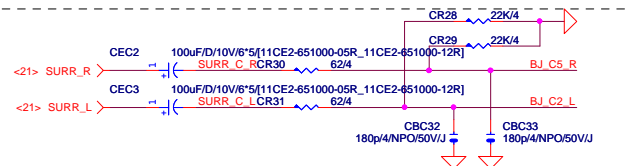
LINE-IN



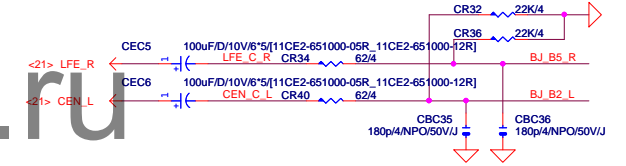
MIC-IN



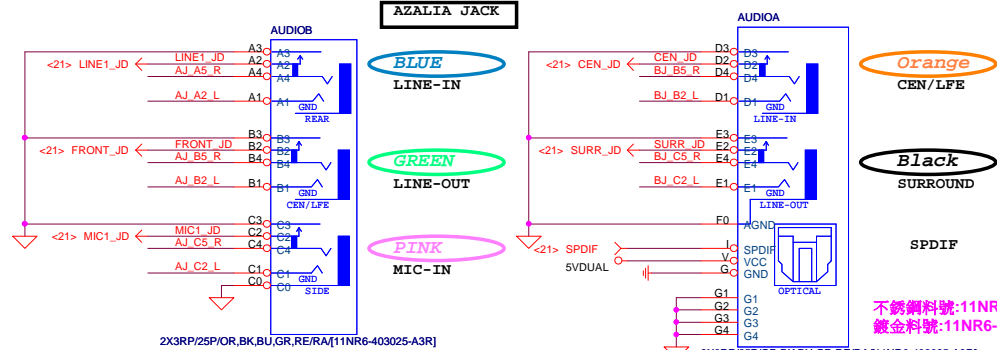
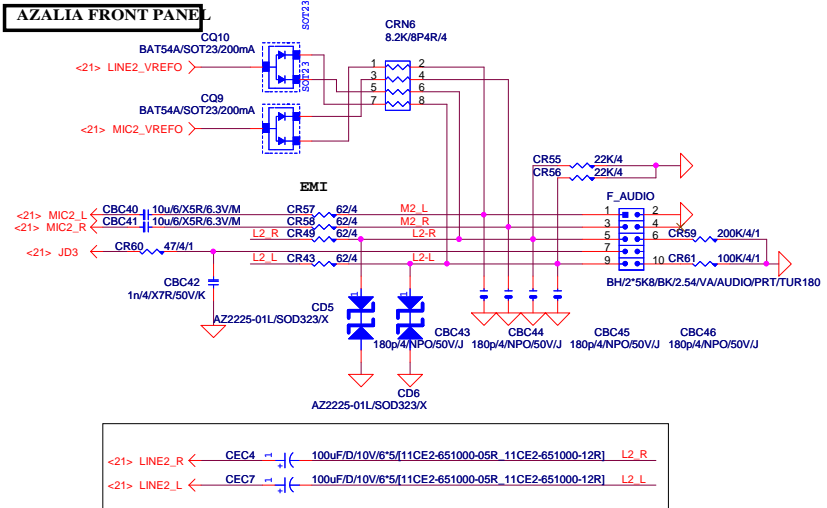
SURROUND



CEN/LFE



AZALIA FRONT PANEL

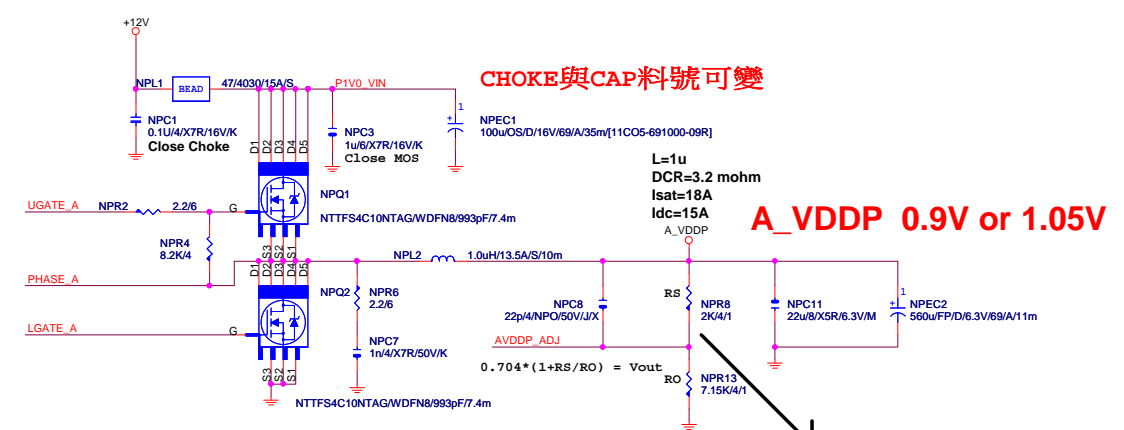
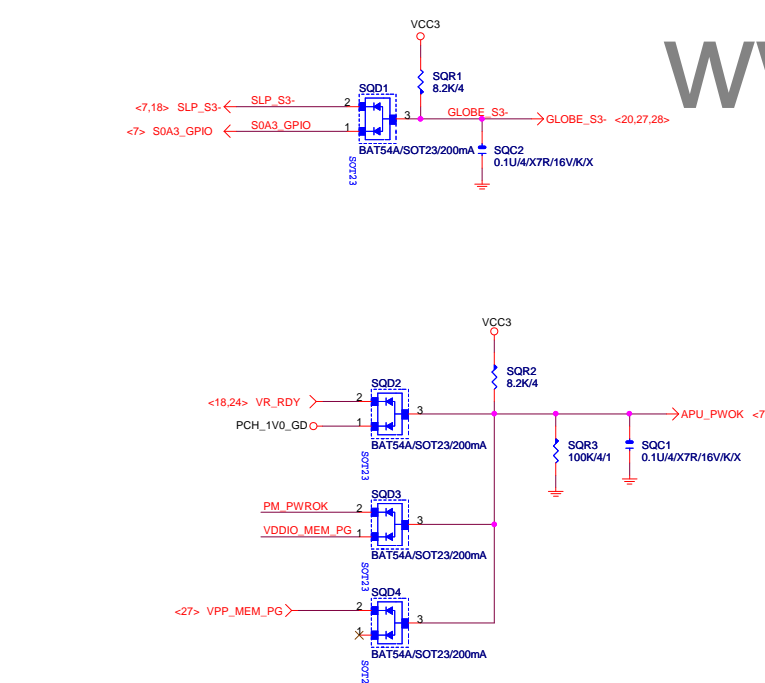
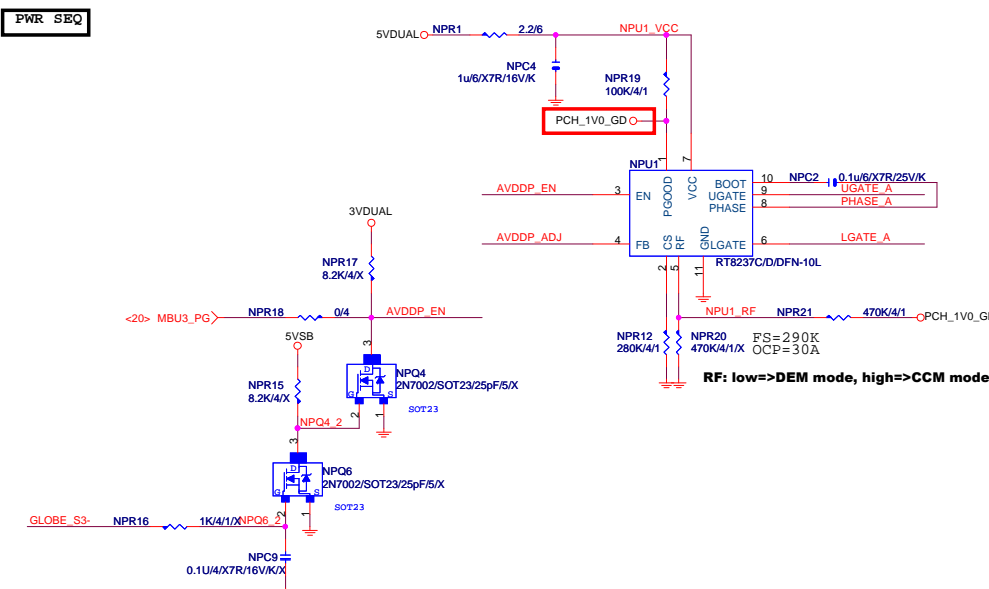


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鍍金料號:11NR6-403025-92R

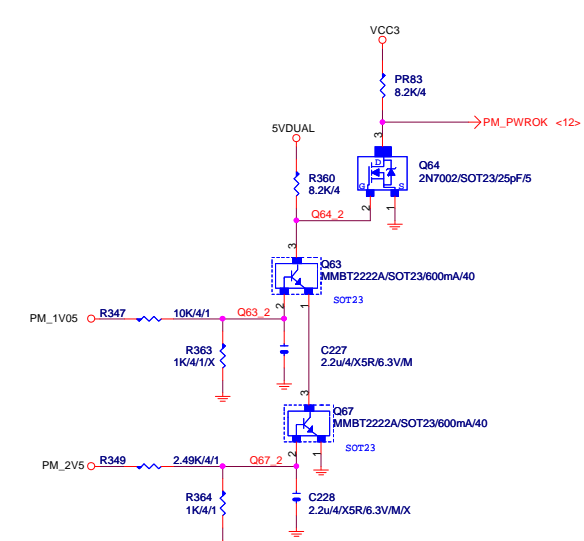
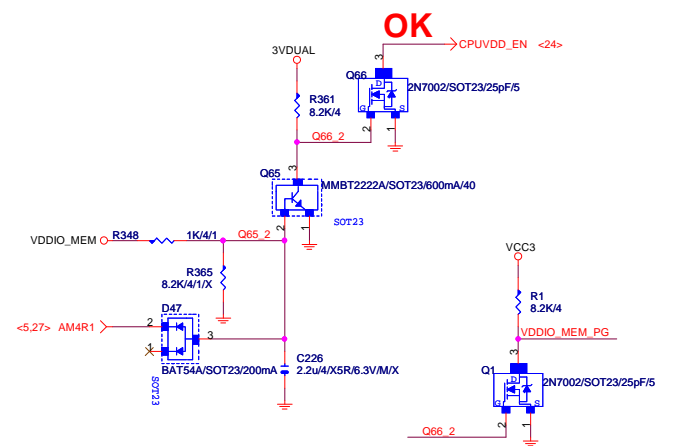
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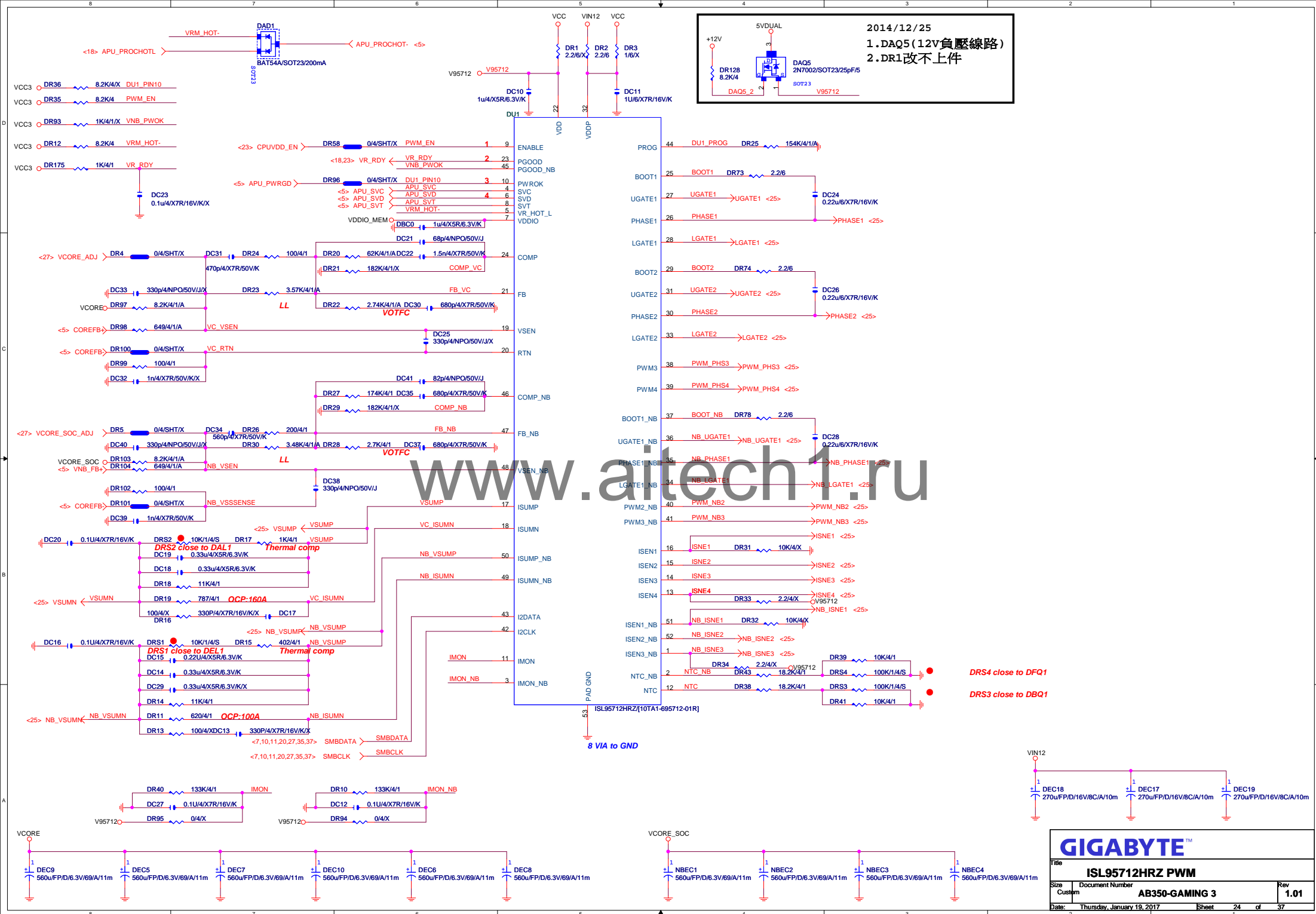
AUDIO JACK

Title	Document Number	Rev
Size	AB350-GAMING 3	1.01
Custom		
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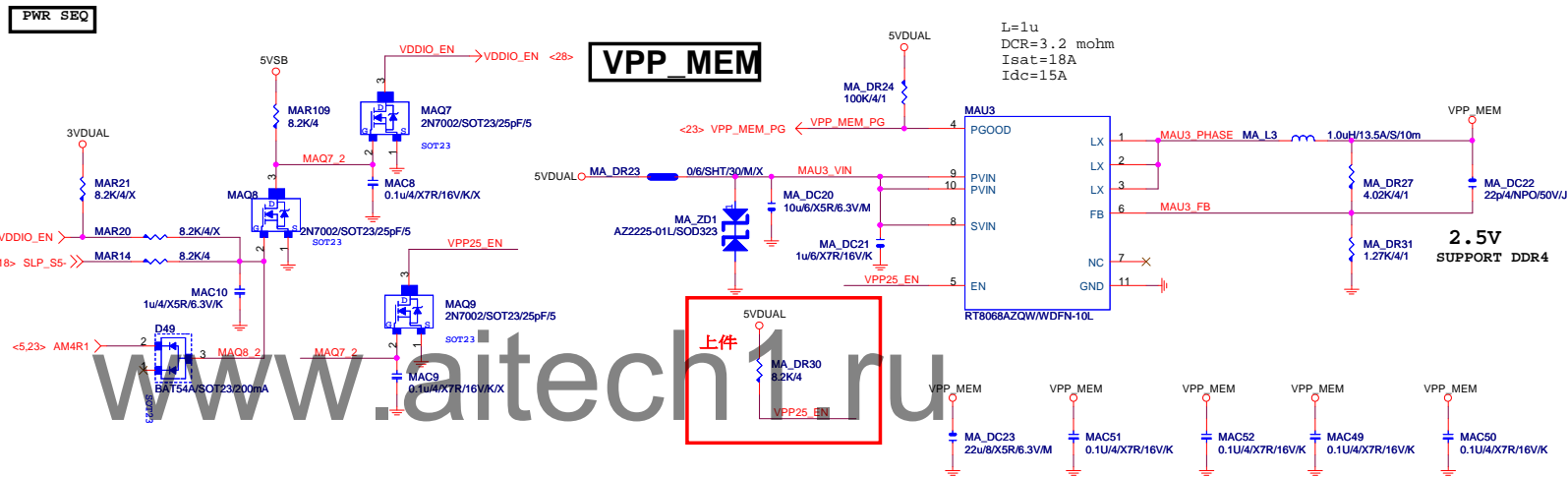
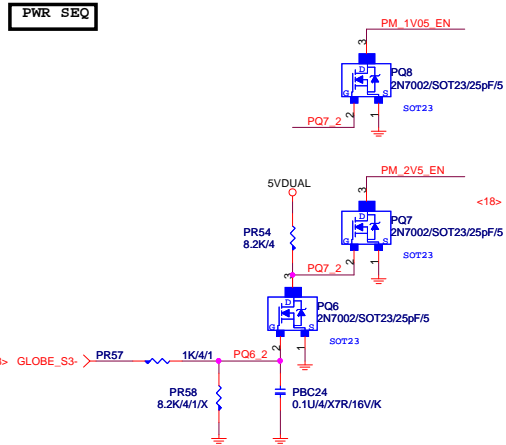
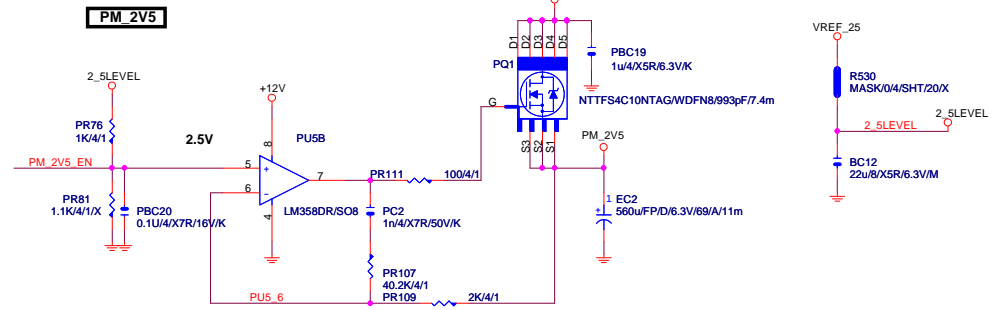
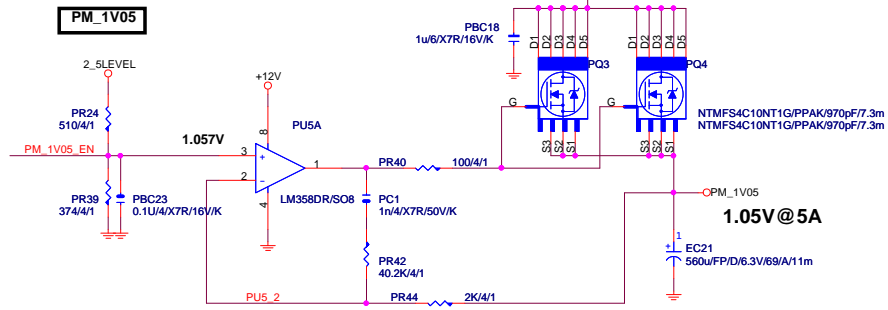


CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V



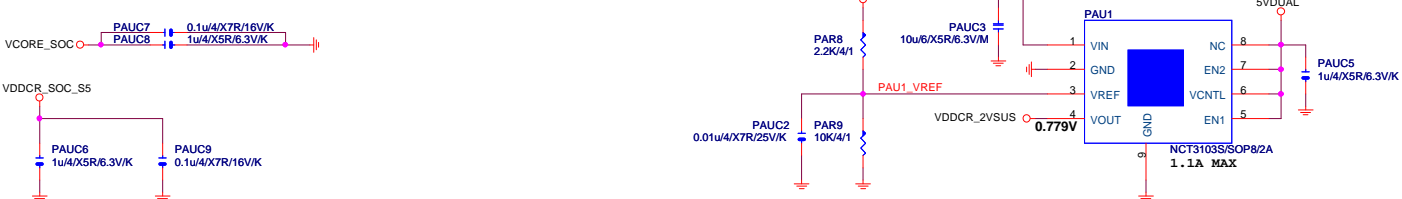
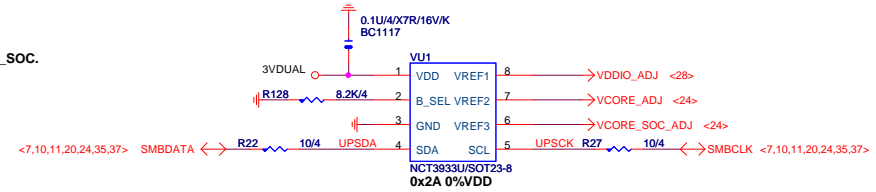
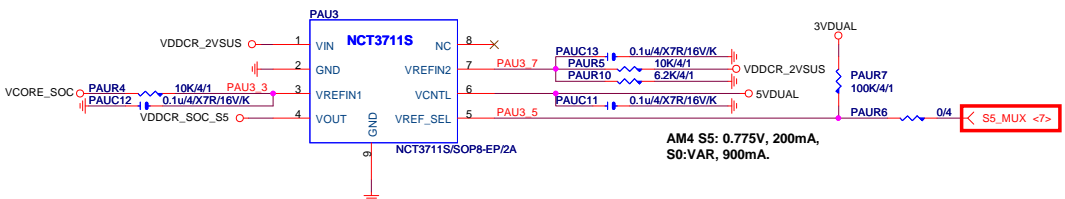


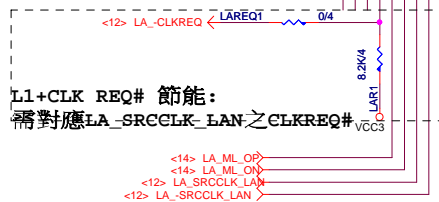
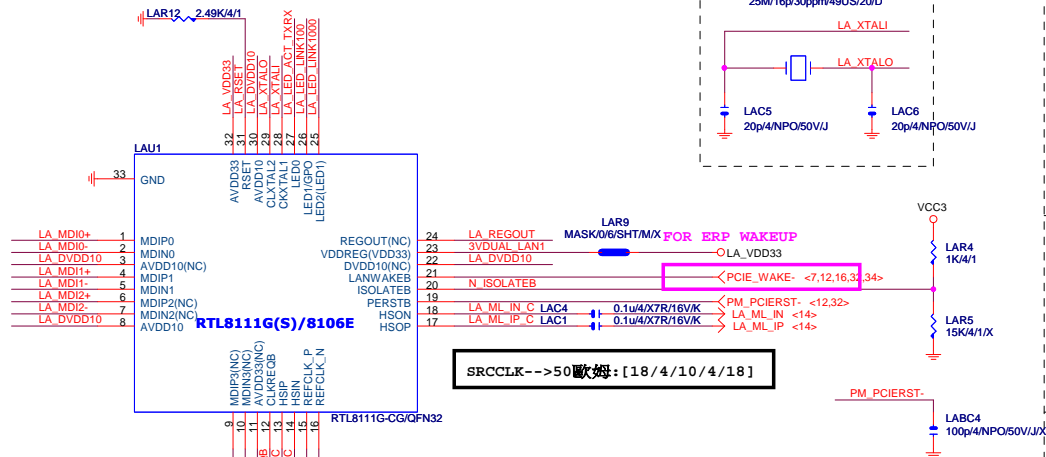




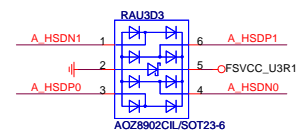
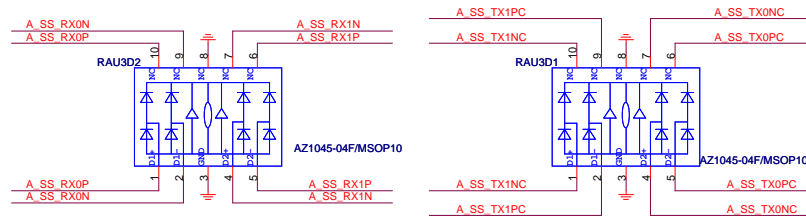
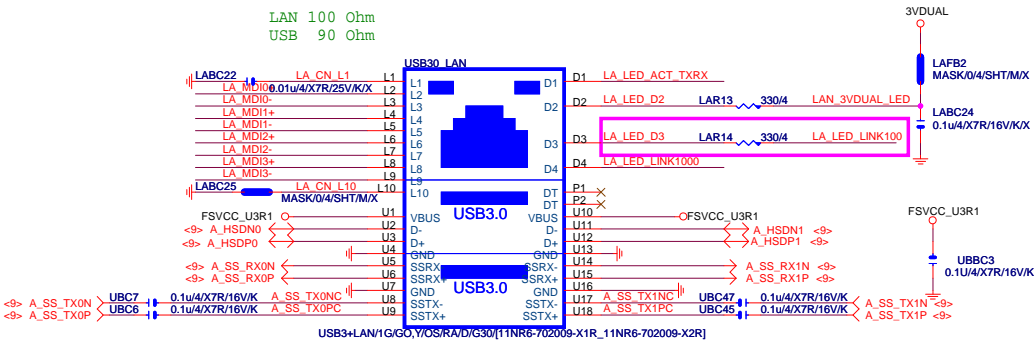
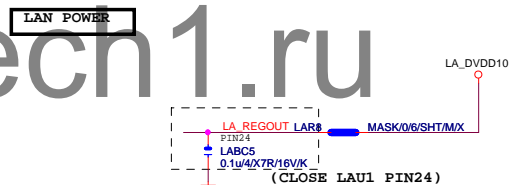
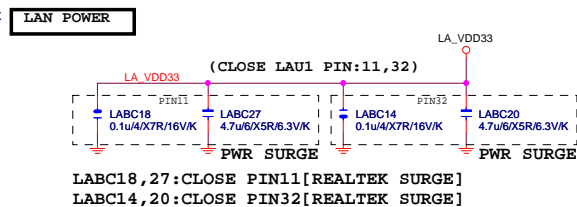
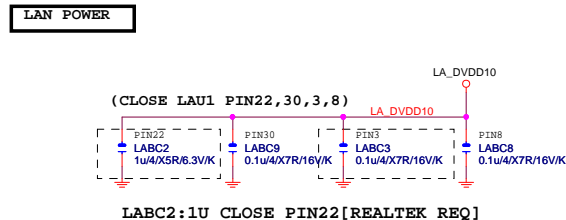
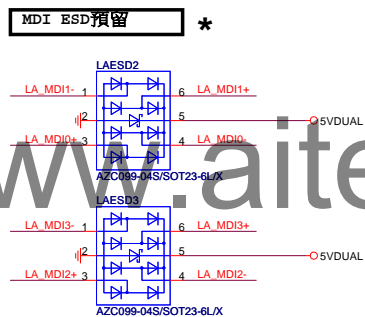
VDDCR SOC S5

S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCORE_SOC.
L: If VCORE_SOC < 0.775V (OR 0.85V), VDDCR_SOC_S5=0.775V.
If VCORE_SOC >= 0.775V (OR 0.85V), VDDCR_SOC_S5 will trace VCORE_SOC.



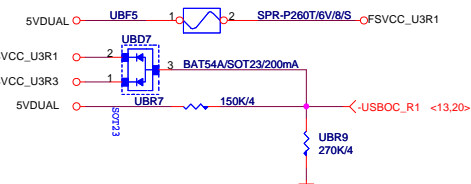


LA_ ML-->80歐姆:[15/5/5/5/15]



EMI SHORT PAD

PS:視EMI需求





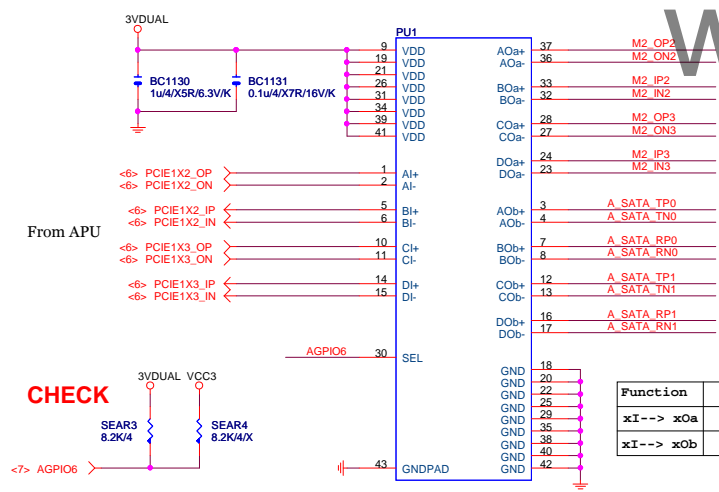
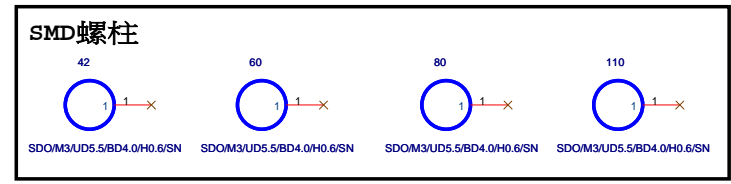
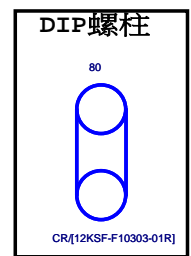
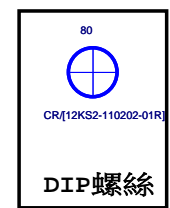
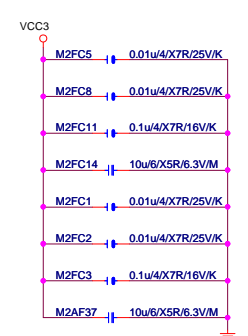
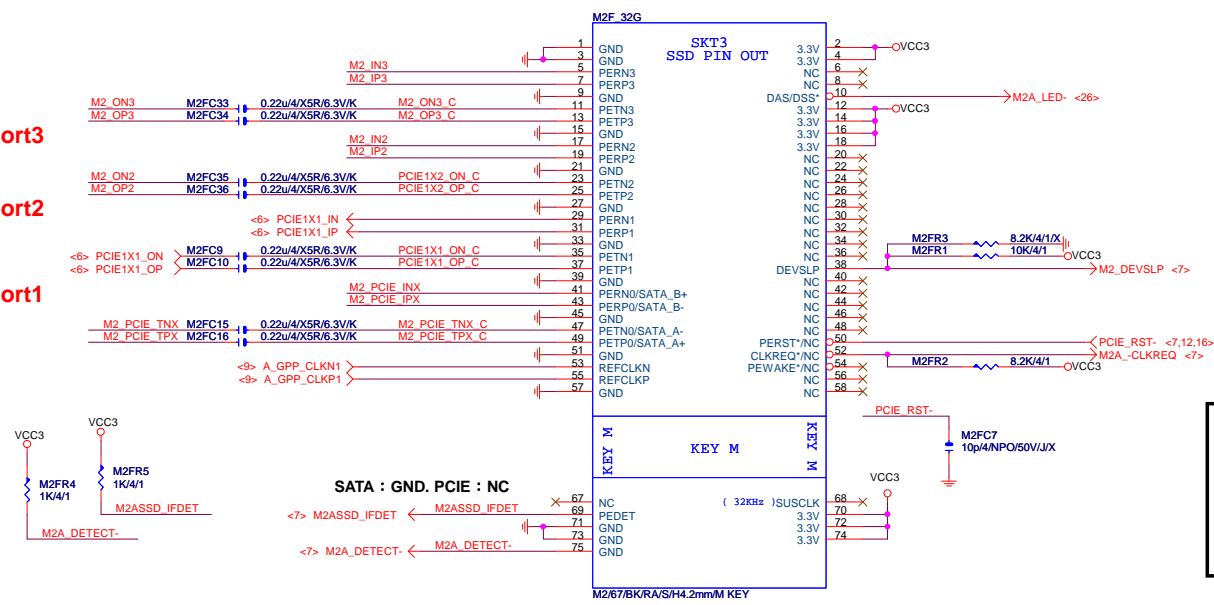
Rev 0.5

M.2 Lane4 from AM4 port3

M.2 Lane4 from AM4 port2

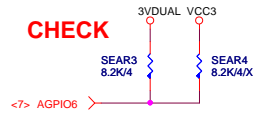
M.2 Lane4 from AM4 port1

by SWITCH Select



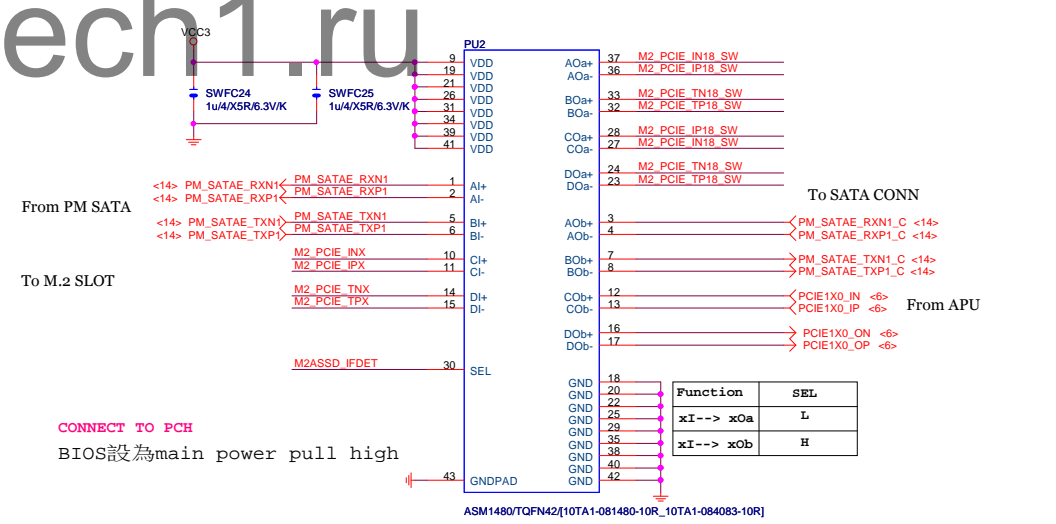
To M.2

To SATA CONN



PCIE GEN3 SW CBTLO4083BBS/HVQFN32[10TA1-081480-10R_10TA1-084083-10R]
GEN3 :CBTLO4083BBS/HVQFN32[10TA1-084083-10R]

Function	SEL
xI--> xOa	L
xI--> xOb	H



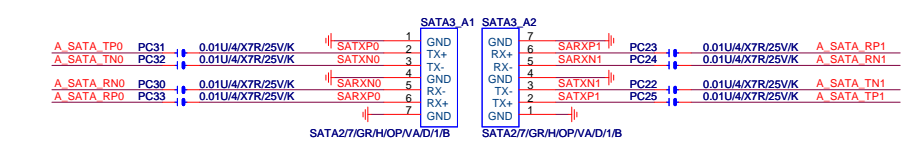
From PM SATA

To M.2 SLOT

CONNECT TO PCH
BIOS設為main power pull high

To SATA CONN

Function	SEL
xI--> xOa	L
xI--> xOb	H

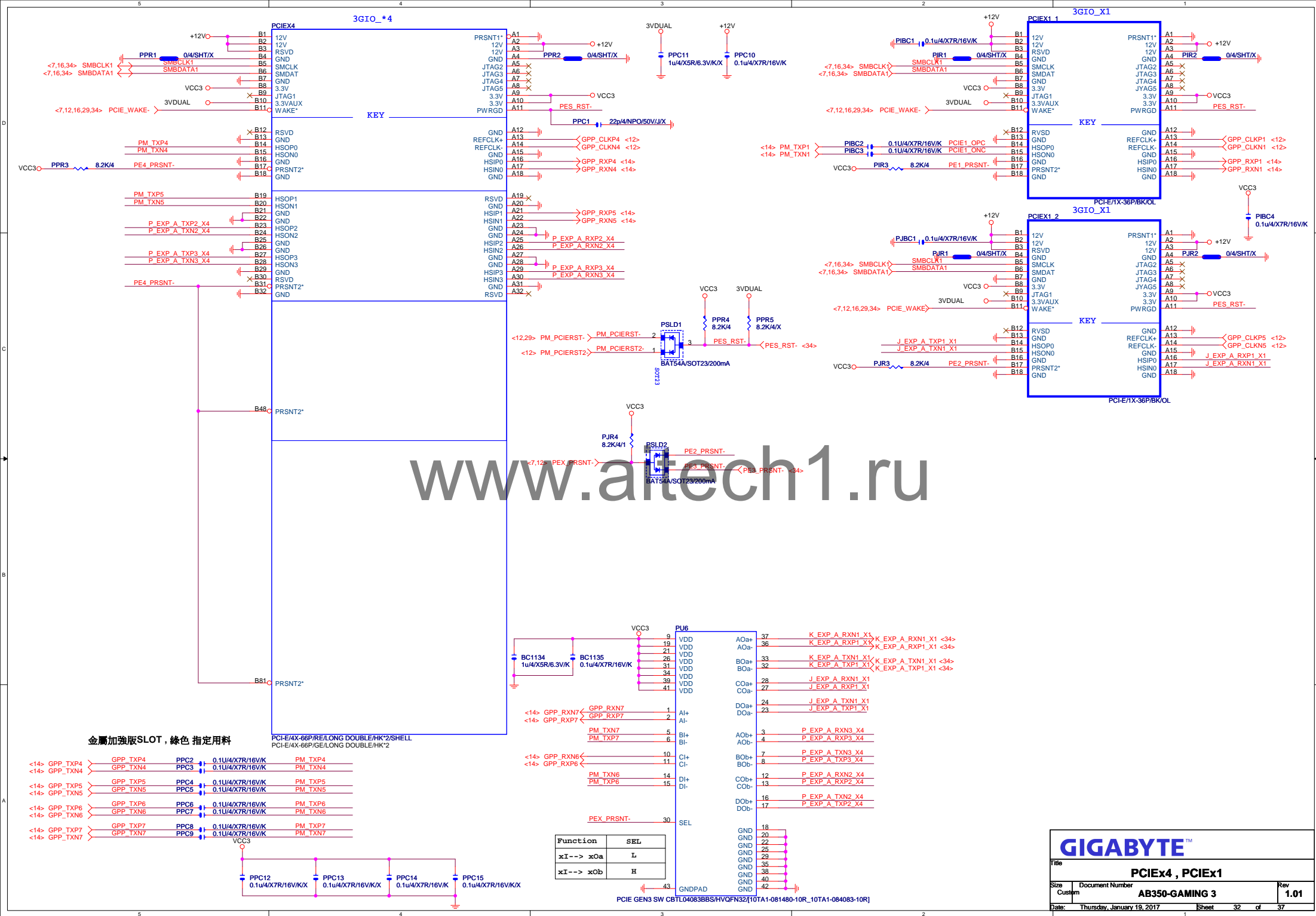


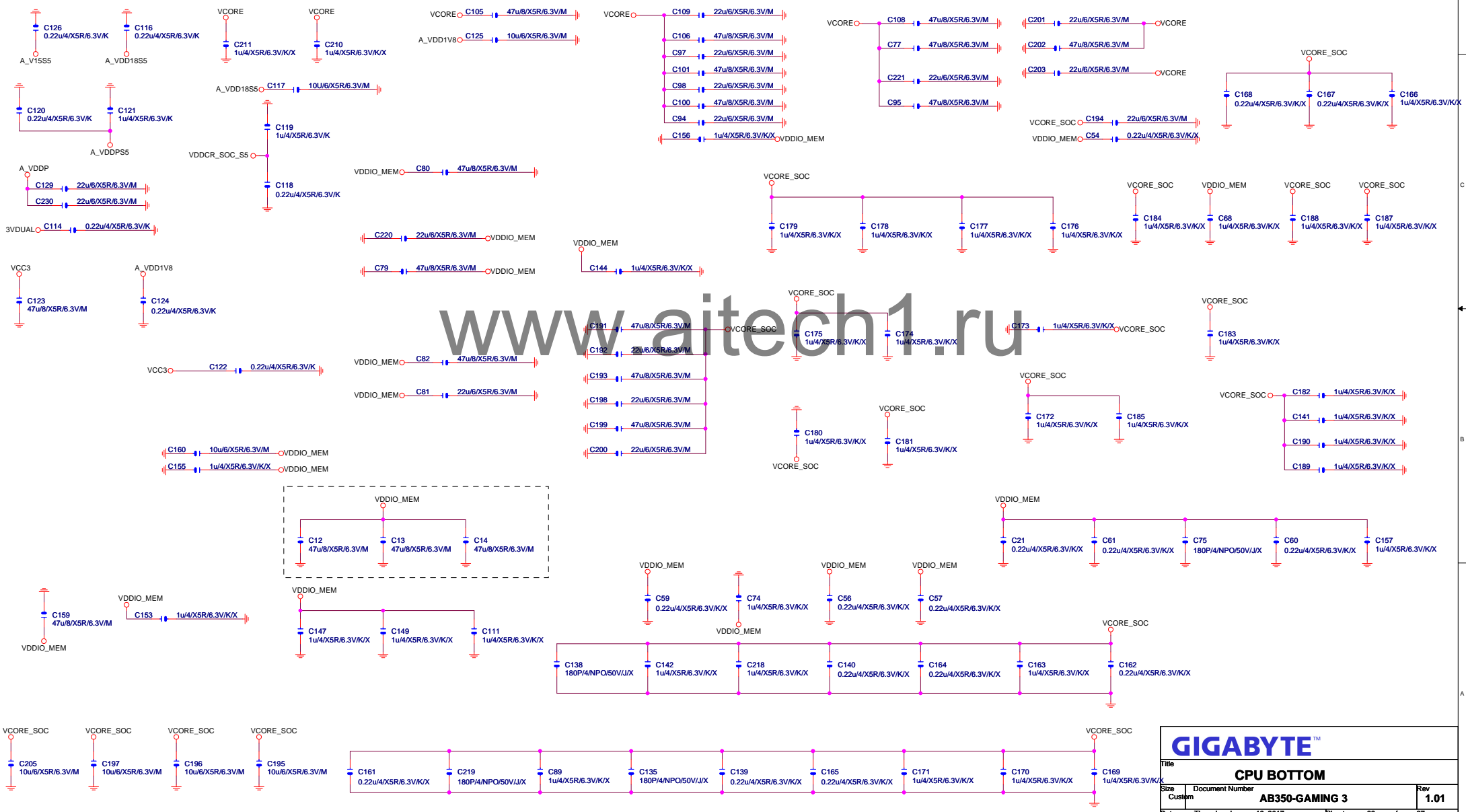
GIGABYTE™

Title**M.2 SWITCH**

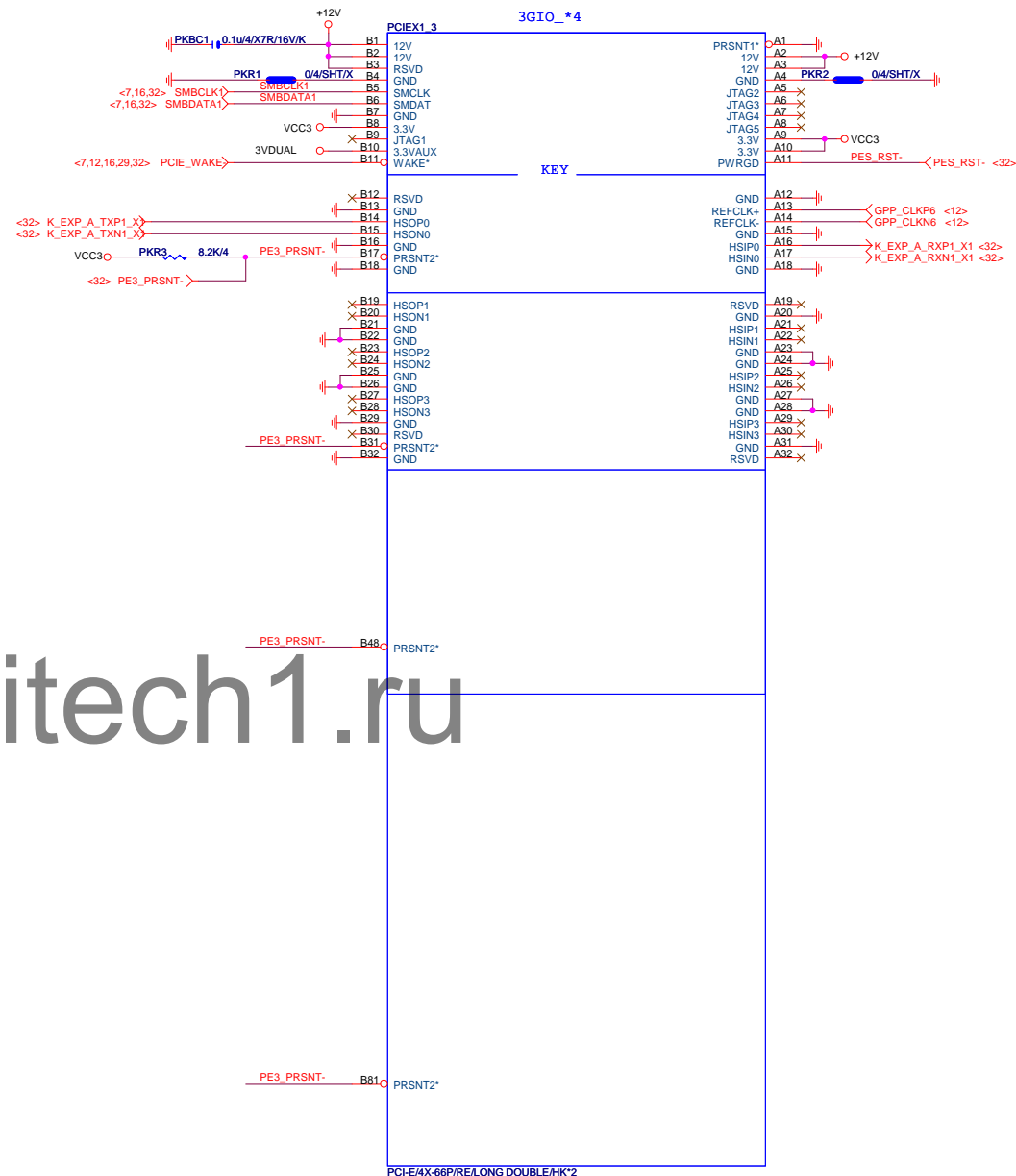
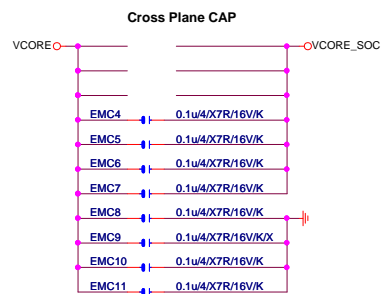
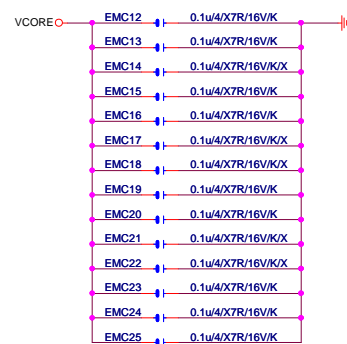
Size CustomDocument Number**AB350-GAMING 3**Rev**1.01**

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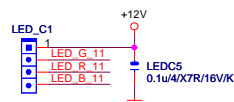
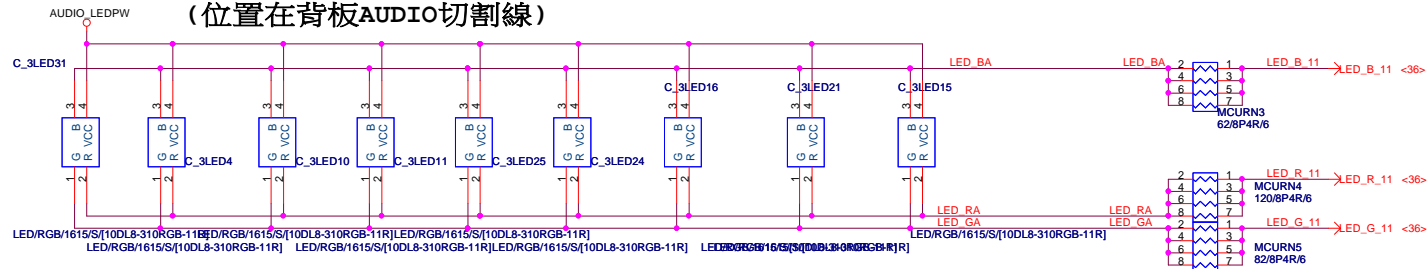
CPU TOP CAVITY



第一區 LED

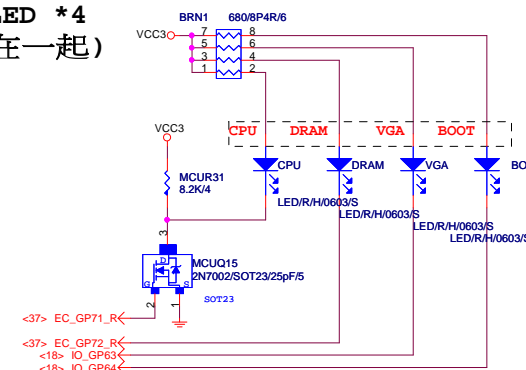
Rev 0.63

FOR AUDIO 正發光 LED*40
(位置在背板AUDIO切割線)

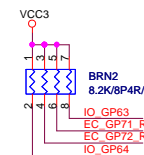


PH/1*4/BK/2.54/VA/D/[11NH2-000104-E1R]

DEBUG PORT LED *4
(位置需擺放在一起)



用文字面表示

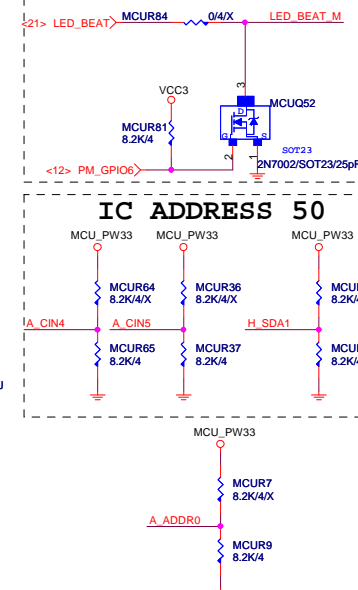
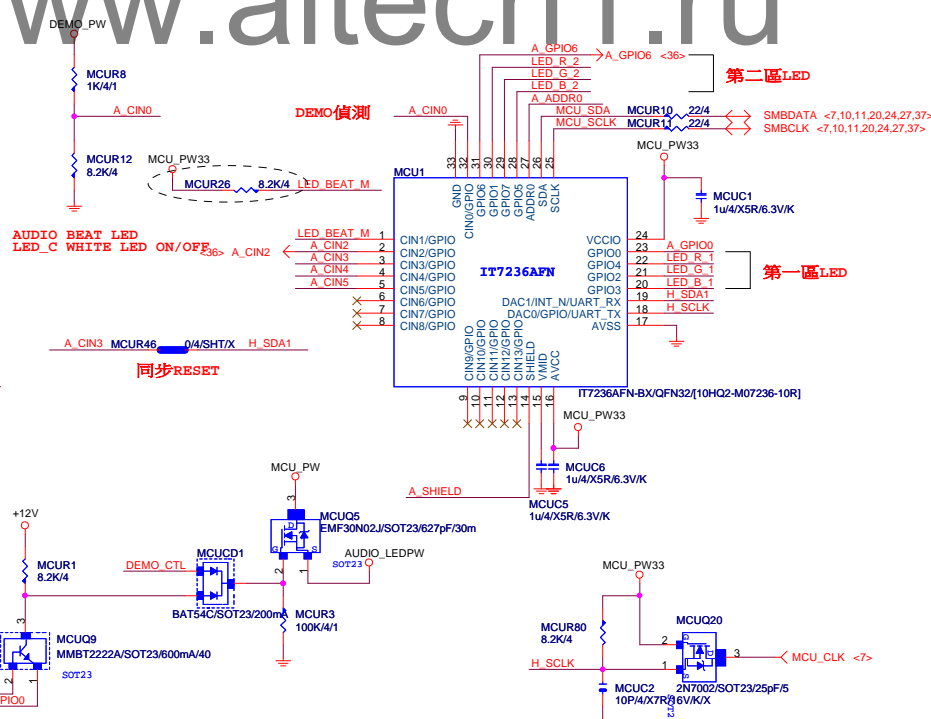
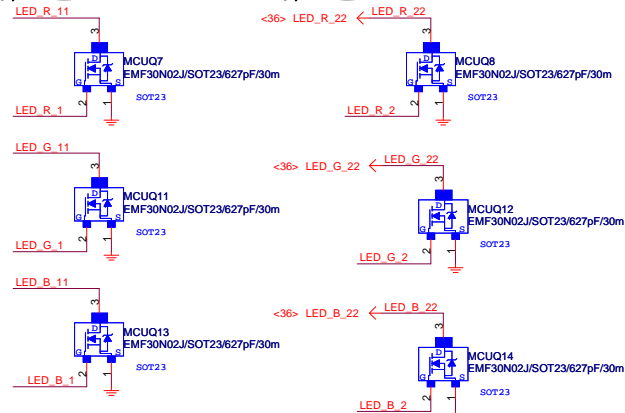


LED GPIO PIN DEFINE

EC_GP71_R	CPU DEBUG
EC_GP72_R	DDR DEBUG
IO_GP63	VGA DEBUG
IO_GP64	BOOT DEBUG
PM_GPIO5	LED_C LED SWITCH

第一區 LED CONTROL

第二區 LED CONTROL



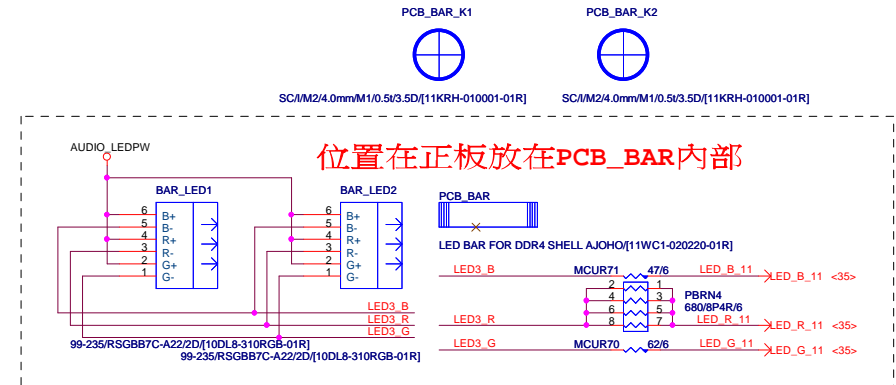
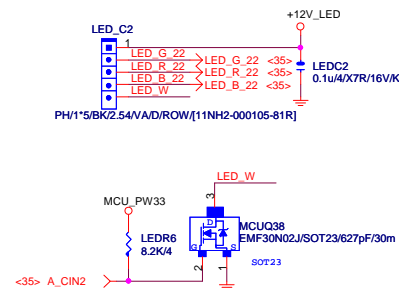
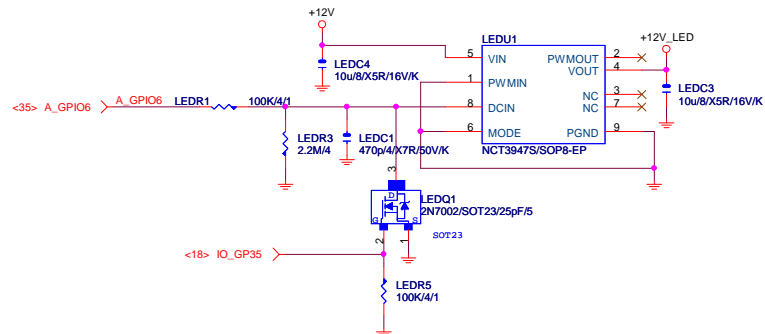
Note : Pulldown address is 0x8C

GIGABYTE

CPU / AUDIO / PCIE/REAR LED

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